Speedups from extending embedded processors with a high-performance coarse-grained reconfigurable data-path

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Abstract

In this paper, an embedded system that extends microprocessor cores with a high-performance coarse-grained reconfigurable data-path is introduced. The data-path have been previously introduced by the authors. It is composed by computational resources able to realize complex operations which aid in improving the performance of time critical application parts, called kernels. A compilation flow is defined for mapping high-level software descriptions to the microprocessor system. The kernel code is mapped using a properly developed mapping algorithm for the reconfigurable data-path, while the non-critical segments are executed on the microprocessor. Extensive exploration is performed by mapping four real-life applications on six different instances of the system. The results show that the speedup from executing kernels on the reconfigurable logic ranges from 6.3 to 154.3, relative to the software execution on the processor since the available processing elements of the data-path are efficiently utilized. Important overall application speedups, due to the kernels’ acceleration, have been reported for the four applications. These overall performance improvements range from 1.70 to 3.70 relative to an all-processor execution. Furthermore, the experiments show that the proposed data-path achieves faster kernels’ execution compared with other high-performance data-paths.
Keywords: Reconfigurable embedded systems; Coarse-grained reconfigurable data-path; Performance;
Compilation flow; Scheduling