Using on-chip networks to implement polymorphism in the co-design of object-oriented embedded systems

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Abstract

The Network-on-Chip (NoC) paradigm brings networks inside chips. We use the routing capabilities inside NoC to serve as a replacement for Virtual Method Table (VMT) for Object-Oriented (OO) designed hardware/software co-design systems where some methods could be implemented as hardware modules. This eliminates VMT area and performance overhead in OO co-designed embedded systems where resources are limited and where some functionality needs to be implemented in hardware to meet performance goals of the system. Our experimental results on real world embedded applications show up to 32.15\% lower area and up to 5.1\% higher speed compared to traditional implementation using VMT.

Keywords: Embedded systems; Object-oriented design; Network-on-chip (NoC); Hardware–software co-design; Polymorphism; Virtual method dispatch; Application-specific instruction processor (ASIP)