A high-level requirements engineering methodology for electronic system-level design

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Abstract

Current electronic systems’ complexity severely limits their validation. Even if development frameworks keep improving and are heavily supported by the industry, methods for hardware/software electronic systems co-design are reaching a major crisis. Although the community is heading towards higher abstraction levels, requirements remain out of the validation scope. We therefore present a requirements engineering methodology that intersects formal, linguistic, and scenario views. Modeling consists in abstracting functionalities’ behaviours in terms of actions, expressed in a semi-formal structured language, later automatically translated in a pure formal notation. Such a mix makes the language accessible to designers and permits automation. Validation is then performed using consistency rules. Finally, an elicitation of missing functionalities is achieved using Boolean algebra.

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