Dependable design technique for system-on-chip

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Abstract

A technique for highly reliable digital design for two FPGAs under a processor control is presented. Two FPGAs are used in a duplex configuration system design, but better dependability parameters are obtained by the combination of totally self-checking blocks based on a parity predictor. Each FPGA can be reconfigured when a SEU fault is detected. This reconfiguration is controlled by a control unit implemented in a processor. Combinational circuit benchmarks have been considered in all our experiments and computations. All our experimental results are obtained from a XILINX FPGA implementation using EDA tools. The dependability model and dependability calculations are presented to document the improved reliability parameters.

Keywords: Reliable digital design; FPGA; Dependability model; Dependability calculations; On-line testing; Fault security; Self-testing; Totally self-checking; Single even upset; Reconfiguration

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